Clean Version of Pending Claims

GTL + DRIVER
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Serial No.: 09/620,679

7.   [AMENDED] A method of communicating data in an integrated circuit using internal interconnects, the method comprising:

receiving a data signal;

adjusting a first resistance coupled to a first supply voltage, based on a manufacturing process, the first supply voltage and a temperature;

adjusting a second resistance coupled to a second supply voltage, based on the manufacturing process, the first supply voltage and the temperature; and

adjusting a third resistance coupled to the second supply voltage, based on the manufacturing process, the first supply voltage and the temperature; and

wherein the first resistance, second resistance and third resistance are each individually adjustable.

8.   A method of communicating data in an integrated circuit using internal interconnects, the method comprising:

selecting a resistance of a divider network based on a manufacturing process, a supply voltage and a temperature;

selecting an edge rate of a driver coupled to the divider network, the selected edge rate based on the manufacturing process, the supply voltage and the temperature;

receiving a data signal; and

providing an output based on the data signal, the resistance, and the edge rate.

9.   The method of claim 8 wherein selecting an edge rate of a driver coupled to the divider network comprises maintaining a substantially constant edge rate.

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10.   The method of claim 8 wherein providing an output comprises turning on a PFET transistor and turning off an NFET transistor.

11.   The method of claim 8 wherein selecting a resistance of a divider network comprises selecting a plurality of parallel resistance elements.

12.   The method of claim 8 wherein selecting a resistance of a divider network comprises executing programming for selecting resistance elements from a plurality of switchable resistance elements.

13.   The method of claim 8 wherein selecting an edge rate of a driver coupled to the divider network comprises selecting a plurality of parallel resistance elements.

14.   The method of claim 8 wherein selecting an edge rate of a driver coupled to the divider network comprises executing programming for selecting resistance elements from a plurality of switchable resistance elements.

15.   The method of claim 8 further comprising:
       receiving a tristate enable signal; and
       actuating a switchable resistance element in response to the tristate enable signal.

16.   The method of claim 15 wherein actuating a switchable resistance element comprises actuating a programmable inverter.

23.   The method of claim 7 wherein adjusting a first resistance includes changing a resistance of a semiconductor.

24.   The method of claim 7 wherein adjusting a first resistance includes changing a gate voltage on a field effect transistor (FET).

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25.   The method of claim 7 wherein adjusting a first resistance includes selecting a predetermined number of programmable bits from a plurality of programmable bits.